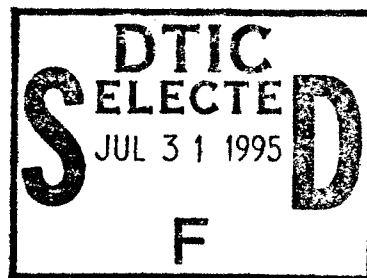


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# FREE SPACE OPTICAL MEMORY BASED ON VERTICAL CAVITY SURFACE EMITTING LASERS AND SELF-ELECTRO- OPTIC EFFECT DEVICES

James M. Battiato, (RL); Thomas W. Stone,  
(Wavefront Research); Miles J. Murdocca,  
(Rutgers University); Rebecca J. Bussjager,  
(RL); Paul R. Cook, (RL)



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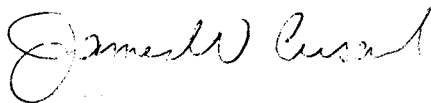
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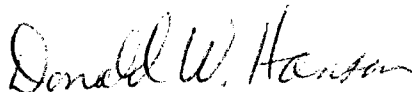
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The authors contributed as follows: James Battiato authored this report and led the effort. Thomas Stone aided in optical system set up. Miles Murdocca aided in designing the overall architecture. Rebecca Bussjager aided in optical system set up. Paul Cook aided in electronic design and fabrication.

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## 1.0 INTRODUCTION

The potential advantages that optics may provide for free space parallel processing systems are generally well known.<sup>1</sup> Among them are massive parallelism, freedom from capacitive loading and mutual interference effects, large fan-outs, and the ability to cross optical signals without interference. In an attempt to exploit these advantages, a general model (Figure 1) has evolved in which cascaded arrays of optical logic gates or smart pixel devices are interconnected optically in free space. At each processing plane, binary 1's and 0's are created by modulating the intensities of the free space optical signals. Optical interconnects then guide these signals to successive planes.

Several successful demonstrations based on this model have incorporated the symmetric self-electro-optic effect device (S-SEED).<sup>2</sup> S-SEEDs consist of two SEEDs connected in series. Device inputs and outputs are both composed of a pair of beams, with each input beam focused on a SEED window. In this symmetric configuration, one SEED window is in a high reflectivity state, while the other is in a low reflectivity state. If the power of both of the input beams is equal, the state of the S-SEED is read-out and remains unchanged. If, however, the high reflectivity window is illuminated with more power than the low reflectivity window it is connected to, the state of the S-SEED toggles with the reflectivities of the windows interchanged. Free space optical parallel processing systems utilizing S-SEEDs have demonstrated basic digital logic,<sup>3</sup> photonic switching,<sup>4</sup> and image processing functions.<sup>5</sup> A common aspect of these systems is the method used to address the S-SEED arrays. Typically a single source array generator is used to produce the necessary optical power.

An alternative approach to array generation investigated here is the use of vertical cavity surface emitting laser (VCSEL)<sup>6</sup> arrays. Advantages of using VCSELs in place of traditional optical array generators in free space optical parallel processing systems are considered in Section 2 and the resulting impact on system architecture is discussed in Section 3. An experimental demonstration of a microlaser based scroll processor is discussed in Section 4. In this experiment, VCSELs provide optical setup power for S-SEEDs and can with modifications ultimately provide readout power as well. Conclusions follow in Section 5.

## **2.0 MICROLASER BASED ARRAY GENERATION AND INTERCONNECTS**

### **2.1 Spot Array Generation**

Array generators are used to address optical logic gates or smart pixel devices. Although requirements vary with each specific application, qualities desirable of array generators usually include: 1) uniform beam intensity; 2) high efficiency; 3) capability of producing large arrays; and 4) reconfigurability. Traditionally, optical power supplies have been created by using array generators which take a single input beam and divide it into an array of multiple output beams. Many techniques for producing optical power supplies of this type have been reported.<sup>7</sup> These techniques include the use of microlens arrays, holography, Dammann gratings, and cascaded beamsplitter approaches( such as the cascading of birefringent slabs).<sup>8</sup> Although each of these techniques possesses unique design tradeoffs, there is an important performance characteristic common to all of them. When a single source is distributed with an array generator, the power per pixel decreases as array size increases. This creates a tradeoff between system size and speed when used in systems based on SEEDs, or other similar devices, where device switching speed is typically proportional to input optical power. For example, if a  $N \times N$  array of devices is

powered by a such an array generator, the power delivered to each device (neglecting losses) is equal to the power of the single laser source divided by  $N^2$ . As  $N$  becomes large the power delivered to each device becomes small, decreasing the switching speed of each device as well as that of the overall system. This effect may be offset by using a higher power laser source with the array generator. For the given example of S-SEED devices, finding a compact, scalable, single frequency 850 nm laser source is difficult. This has resulted in increased interest in other methods of array generation.

## 2.2 Microlaser Based Power Supplies

VCSEL devices have enjoyed a rapid development in recent years. VCSELs operate according to the same basic principles as ordinary semiconductor lasers with the exception that the orientation of a VCSEL laser cavity is orthogonal to that of a traditional edge emitting semiconductor laser. As a result VCSELs may be fabricated in compact, individually addressable, two-dimensional arrays which provide circular output beams. Modulation frequencies on the order of a gigahertz have been reported.<sup>9</sup>

One of the many suggested uses for VCSELs has been spot array generation.<sup>10 11</sup> Although tradeoffs exist between using VCSELs and traditional single source spot array generators, VCSELs permit flexibility in the design of interconnects and system architectures not offered by the sole use of non-addressable spot array techniques. For example, non-addressable spot array techniques inherently produce arrays in which all the pixels are enabled simultaneously. As a result, masking planes or external SLM's are sometimes required to disable the outputs of unwanted interconnects. An individually addressable microlaser array, on the other hand, may act as both an array generator and a spatial light modulator allowing the interconnect masks to be mapped directly into the modulation of individual microlasers. Thus, instead of producing an entire array of spots,

microlasers powering unwanted interconnects are simply not powered during readout. In the same manner, this simple scheme can be extended to allow for reconfigurable interconnects if a host controller is used to control each microlaser or subarray of microlasers. Then, the interconnect masks can be reconfigured dynamically by selectively disabling microlasers.

For the given example of S-SEEDs, the devices must be preset to function as logic gates. Presets are accomplished by optically setting the S-SEED into either a high or low state, depending on which Boolean logic operation is desired<sup>3</sup>. When illuminated by a single source array generator, an entire array of S-SEEDs is automatically preset to the same logic state. If a VCSEL array generator is used instead, the ability to selectively enable or disable microlasers provides the ability to spatially vary device presets across a single S-SEED array. If one microlaser is used to drive each S-SEED window, then every S-SEED on the array may be preset independently of its neighbors. This technique is discussed in more detail in Section 4. Also, the impact of spatially varying presets and reconfigurable masks on system architecture are addressed in Section 3.

A non-addressable spot array technique may be combined with a separate spatial light modulator to produce the same effects discussed above, but with added complexity. Matching the pitch of the spots produced by the array generator, for example, to that of the devices they are illuminating becomes more complicated when the spatial light modulator pixel dimensions are different from those of the spot array generator or the device array. Transmission losses through the spatial light modulator, alignment errors, and decreased contrast performance are also limitations of this approach. In comparison, VCSELs provide gain and perhaps can be used with an infinite contrast ratio with the 0 logic state being represented by an unpowered microlaser (zero intensity). In practice, however, it might be advantageous to represent the logic 0 state by microlasers driven just



under lasing threshold, from where the modulation speed may be increased at the expense of a finite (but large) contrast ratio. Such switching speeds are also significantly faster than other spatial light modulators. A possible disadvantage, however, of using microlasers for power beams is that any temporal skew in the turn-on times of the lasers (neglecting jitter) can result in erroneous transient switching of the devices they are powering. This places a burden on the driving electronics of the microlaser to minimize skew across the array. Traditional array generators do not suffer from this problem since the spots are formed from a single laser source which causes all spots in the array to turn on and off simultaneously with the source. The microlaser technique is also susceptible to fluctuations in the outputs of the individual microlaser in an array. In this respect traditional array generators offer better performance since any fluctuations in the laser source are experienced in the same way by each pixel in the spot array. On the other hand, introducing microlaser control provides the possibility of trimming the individual devices to obtain the desired uniformities or alternatively tuning the device intensities to compensate for field-based losses (e.g. vignetting and surface reflections). Thermoelectric cooling of the microlaser arrays can increase laser stability and may help to minimize this problem.

As discussed earlier, the availability of a laser source which can scale in power as system size and/or speed increases is a limiting factor of the single source beam generation method. The use of VCSEL arrays as optical power supplies can, in principle, diminish this scalability problem. Each individual pixel in a VCSEL array supplies its own light independently of array size. Thus the dimensions and number of devices in a microlaser array (within heat dissipation and fabrication constraints) can be increased without diminishing the available power per pixel. They are also not subjected to losses typical of single source array generators. The extent of scalability offered by VCSEL based array generators, however, is bounded by device limitations. For example, thermal problems

and electrical contact difficulties limit current array sizes. Until these problems are overcome, larger spot arrays may be generated by combining traditional array generators with VCSELs to increase spot density through sub array generation techniques<sup>8</sup>.

Another important consideration is the coherency of the spots in an array. Traditional array generators formed from the same source create beams which are coherent with respect to each other. Thus when spots are combined interference effects occur unless the polarization of the combined spots are made orthogonal to each other. In the case of microlaser array generators, each of the individual lasers in the array can be made incoherent with respect to its neighbors. Thus it is not necessary to use polarization techniques to reduce interference effects.

Polarization properties of VCSEL arrays are a concern, however. Beam polarization may vary across an array of microlasers causing problems in systems that do use polarization optics for beam steering. This can be avoided if a polarizer is placed directly after the array, but there is an obvious penalty in power for this type of correction. Other potential limitations involve the onset of higher order lasing modes with increases in drive current which can affect imaging within a system. Laser lifetime is also an important consideration which affects system reliability. These problems are currently areas of active device research and may be corrected through fabrication techniques.<sup>12 13</sup>

### **3.0 Architectural Considerations**

#### **3.1 Introduction**

The impact of microlasers on system architecture may be better understood by examining not only systems which employ them, but those that did not as well. The model of the original S-SEED based processor developed at AT&T Bell Labs in Holmdel, New Jersey,<sup>4</sup> is illustrated in Figure 1. In this model, four cascaded S-SEED arrays are interconnected with regular interconnection patterns in free space. Fixed masks customize the system for specific functions. The system implements a small programmable logic array (PLA). The actual demonstrated function is a 2-to-4 decoder, which is illustrated in Figure 2. The decoder translates a logical encoding on the A and B input lines into a spatial encoding on the  $D_i$  lines in which a different  $D_i$  is high for each AB pattern.

Figure 3 illustrates a circuit diagram of the AT&T 2-to-4 decoder. A functionally equivalent electronic circuit diagram for a 2-to-4 decoder is shown in the figure. In comparison, the gate count for the S-SEED decoder appears exceptionally high for such a simple four-gate electronic function, which is a result of the experimental setup and is not fundamental to the methods<sup>3</sup>. For example, every signal must travel through a NOR gate on every level, which means that a relative inversion is not possible since every signal goes through the same number of inverting logic gates relative to every other signal. Since a relative inversion cannot be made between two signals, dual-rail logic is used, in which a relative inversion is made by swapping bits with a dual-rail bit-pair. This increases gate count by approximately a factor of two over a single-rail approach.

NOR logic is used at every level. Since NOR is a nonassociative function, complex expressions cannot be trivially decomposed as they might be for an associative function like AND or OR. In order to logically NOR three signals A, B, and C, signals A and B are first NORed. The result cannot then be NORed with C, because the resulting function

would be  $((AB)'C)'$ , which is different from the desired function  $(ABC)'$ . After NORing A and B, the result is complemented in a second step by passing it through a NOR gate. This is followed by a NOR with C in the third step, which produces the desired result. Note that C is complemented twice before the third step, which leaves C logically unchanged. This method of dealing with the nonassociativity of NOR increases circuit depth at least one level per function, and possibly more depending on how the decomposition is implemented. Fan-ins and fan-outs are limited to two, which translates to a higher gate count than would be needed for an approach in which greater fan-ins and fan-outs are allowed.

An electro-optical input was not included in the original AT&T system. Inputs are provided by blocking light at the inputs of the top stage of logic devices, which produces dual-rail 0's at the outputs of the first stage. Selective blocking is then used between the first and second stages to achieve a particular input pattern. This method of providing inputs introduces a cost of two additional rows of logic that are not needed if a more sophisticated interface is used.

There is a cost introduced by the fact that all signals travel through a logic gate at every level regardless of whether or not a logic gate is needed. This property of the architecture equalizes delays between levels, similar to the way delays are equalized in a clock distribution network in conventional digital electronics. This might thus be viewed as a benevolent cost, but it is an almost unavoidable cost with a side benefit that may not be needed.

There is also a cost in forcing every level of logic to perform the same function, such as NOR instead of a mixture of AND, OR, or XOR (Exclusive-OR). For a 2-to-4 decoder, this restriction does not affect the overall gate count, but for other applications it can.

Finally, the regular topology of the gate-level interconnection pattern introduces a significant cost in gate count. Although it has been shown by Murdocca et al.<sup>14</sup> that circuit depth and breadth are comparable to conventional electronic approaches for this model, the overall gate count is typically a factor of 4-8 greater than it can be because of the forced regularity. This increase in gate count is balanced somewhat by greater utilization of the logic made possible through gate-level pipelining.

### 3.2 Microlaser Based System

Unlike the four-stage AT&T system, the microlaser based processor is designed to use only two S-SEED arrays as illustrated in Figure 4, and can even use a single S-SEED stage as is the case for the experiment described in Section 4. Individual microlasers control each S-SEED mesa, which gives much finer control over the functions of the logic devices and provides potentially greater optical power as described in Sect. 2.2.

The model shown in Figure 4 consists of two arrays of optical logic gates and two stages of split-and-shift interconnects. The optical logic arrays are controlled by an electronic function generator via mating microlaser arrays. The microlasers perform the functions of the fixed masks. This is a significant change, over previous systems, because it allows the masks to be reconfigured dynamically by selectively disabling microlasers through a host controller. Although the setup time for disabling a microlaser is limited by the speed of the electronic host controller reconfiguration is a relatively infrequent operation for many applications, and so the relatively slow setup time is not necessarily a critical factor for the success of this type of system.

### 3.3. An Optical Storage Application

A conventional RAM consists of an address decoder and a means for storing bits. For our optical RAM, we designed the decoder to perform the same function as in a conventional RAM, but the stored bits are modulated by the microlasers. This variation is used only so that data can be input to the system by an electronic machine (an HP logic analyzer/function generator for this case). This would be replaced by an optical input mechanism in a complete system.

A number of RAM designs were developed for this model. Fig 4 shows one design, in which a fan-in of two and a fan-out of two are used for each S-SEED logic device. In order to disable an interconnection path, the source microlaser for that path is disabled. This disables the second output of the microlaser as a side effect. Thus, every logic gate has either two outputs or no outputs. Some logic gates in Figure 4 appear to have a single output, because those gates have a second output that is imaged off of the array and is therefore not shown.

The circuit shows a 4 (1-bit) word optical RAM. There are two S-SEED arrays in the system: one for NOR, and one for OR. The interconnect from the NOR array to the OR array is a split-and-shift to the right by 1. The interconnect from the OR array to the NOR array is a split-and-shift to the left by 4. In order to pass the outputs of one row to the inputs of the next, the source row S-SEED windows must be illuminated. Some of these beams need to be blocked in order to customize the circuit for a specific function, such as an address decoder for this case. In order to disable the output of a logic gate, we can place a mask in the image plane as in the static approach previously described. In our approach, the outputs are disabled by selectively disabling microlasers.

The four data bits  $d_i$  that are stored in the RAM are modulated by the microlasers that power the logic gates in the positions shown in the diagram. The address bits  $a_i$  are also modulated by microlasers. The one-bit output  $D$  is at the bottom of the diagram. The entire circuit fits into a rectangle that is five logic gates wide by eight logic gates deep, which gives an area complexity of  $5 \times 8 = 40$ .

### 3.4 Fan-outs and Fan-ins Greater Than Two

Figure 5 shows an alternative RAM design in which a fan-in of two and a fan-out of three are used. The circuit depth is reduced to two levels, and the gate count is reduced to 10 (five logic gates wide by two levels deep). As for the previous case, each logic gate has three outputs or no outputs, since interconnections are disabled at the source. In terms of area complexity, the fan-out of three approach is better ( $5 \times 2 = 10$ ). A fan-in of three is also possible, as well as greater fan-ins and fan-outs. As the fan-ins and fan-outs increase, however, the tolerancing requirements on the devices also increase.

A significant design problem was encountered in using fan-ins greater than two. The S-SEED devices consist of two mesas. If the relative intensity of light that is imaged onto one mesa exceeds the intensity on the electrically coupled mesa, then the device switches such that the mesa with the greater intensity absorbs incoming light. During operation, a preset cycle switches the S-SEEDs into a known state, followed by a data cycle in which the devices may switch back to the opposite state if the relative intensities of the incoming beams differ in the opposite way, and finally, a readout phase allows the states of the S-SEED mesas to be read onto the succeeding stage (this is essentially another data cycle, which may need a preset cycle for the succeeding stage depending on how the system is configured).

If a fan-in of three is used, then complex results may occur. For example, if two high beams and one low beam are on one mesa and the complementary beams (two low and one high) are on the coupled mesa, what will happen? We developed truth tables that describe three-input operation, and we found that there is no way to apply presets such that the common logic functions AND, OR, NAND, or NOR could still be performed for ordinary or dual-rail Boolean logic. The functions that we obtain are majority logic gates, which can be thought of as a form of threshold logic gates. In more detail, we assume that when the irradiance on one S-SEED window exceeds that on the other, the reflectivity of the more greatly irradiated window is switched to low, and if the irradiances are equal, then no change is made in the state of the device. Consider first a fan-in of three. There are three input spots imaged on each window of the S-SEED. The left side of Figure 6 shows a truth table for this case. With a fan-in of three the device acts as a "majority gate," in which the output depends only on the majority of the inputs. If two or more inputs are high, then the output is low, and vice versa. Thus the initial or preset value for the gate has no effect on the output.

An interesting case occurs with a fan-in of four, as illustrated in the right side of Figure 6. Here, the devices are again idealized and four spots are imaged on each S-SEED window. Since now there are cases in which equal numbers of inputs will be high and low (e.g., where each window will have two "bright" spots and two "dim" spots), the preset state of the device is important as that state will then dominate. Although we can use principles of threshold logic design here, we did not pursue this approach because it further diminished an already low contrast ratio.

For the simple case in which a fan-in of two is used, an advantage of using the maskless approach is that the functions of the logic gates can be determined on-the-fly, based on the microlaser settings used in the preset cycle. For example, any combination of AND



and NOR gates may be used on an array, or any combination of NAND and OR may be used, without modifying the physical interconnects. We did not take advantage of this capability in the RAM design because the regular structure of the memory only needed alternating stages of OR and NOR gates, but in a more general system, this capability can be significant.

## **4.0 Experimental Demonstrations**

### **4.1 Introduction**

The single S-SEED array architecture and use of VCSELs with symmetric self electro-optic effect devices (S-SEEDs) were studied experimentally by the construction of a demonstration scroll processor with wrap-around. In this testbed the S-SEED windows were addressed individually by vertical cavity microlasers and in parallel (row by row) by edge-emitting semiconductor lasers imaged through a 1-D Dammann grating. Light reflected off the S-SEED windows was fed back onto the same array through a reflective split-and-shift interconnect. The system was designed to be a flexible testbed and was not optimized for throughput or switching speed. The scroll processor was operated by setting the initial states of the S-SEEDs using the VCSELs and then scrolling the data from row to row using the spot arrays. This is described in detail below.

### **4.2 Optical System**

The scroll processor optical system is illustrated in Figure 7. This testbed was built on an Invar breadboard and consisted functionally of three modules: a readout module that produced the parallel readout(power) beams; a preset module that contained an addressable VCSEL array; and a processor module that contained the single S-SEED

array and feedback interconnect. These modules are identified in Figure 7 by the dashed lines.

The readout module consisted of four semiconductor lasers [Spectra Diode Labs 100 mW, 850 nm wavelength] that were combined using beamsplitters so that each illuminated the one-dimensional Dammann grating with a collimated beam of approximately 1 cm diameter. The Dammann grating was fabricated by AT&T (Naperville, Ill.) and produced a 1 x 8 array of spots with 20 mm pitch in the S-SEED plane from each input beam. The telescope was used to adjust the pitch of these spots and consisted of singlets with focal lengths 38 mm and 175 mm for L6 and L7, respectively.

The preset module contained an 8 x 8 VCSEL array manufactured by Bandgap Technologies, Inc. which was a preliminary device with elements emitting in the range of 849-860 nm. The pitch of the devices in the array was 75  $\mu$ m, and this array was imaged (infinite conjugate) onto the 20 mm pitch S-SEED windows using doublet lenses L3 and L4 (each with focal length  $f=100$  mm, separated by approximately 60 mm) as an imaging lens. Diffuse illumination for the S-SEED array was also provided in this module by an 850 nm light emitting diode (LED) that was imaged with the  $f=50$  mm doublet L5. This diffuse light was introduced into the optical train with a pellicle beamsplitter.

Although we could not exactly match the wavelengths of the microlasers to the S-SEEDs, we were able to preset the states of the S-SEEDs. Accurate readout of the devices, however, was not possible for this wavelength range. It is for this reason that the Dammann grating with a laser source matched to the S-SEEDs was used to perform readout. It is anticipated that VCSELs matching the wavelength of S-SEED operation

will be commercially available in the near future eliminating the need for the readout module.

The processor module was built around an array of S-SEEDs (type M4213A) manufactured by AT&T and packaged on a thermoelectric cooler. These devices had a pitch of 20 mm x 40 mm [i.e., 20 mm x 20 mm window pitch] with a 5 mm x 10 mm window dimension. A subarray of 3 rows of 4 devices was used in this experiment. This S-SEED array was placed in the focal plane (infinite conjugate) of a 10X Olympus microscope objective L1 ( $f = 18$  mm) with a numerical aperture  $NA = 0.3$ . A fanout of two split and shift feedback interconnect was formed by mirrors and beamsplitters as illustrated in Figure 7. S-polarized light entered this module through the preset module and illuminated the S-SEED array with circular polarization due to the quarter-wave retarder. The light reflected from the S-SEEDs was then transmitted through the polarizing beamsplitter with P-polarization after a second pass through this retarder. A few percent of this light was then split off by a pellicle beamsplitter and imaged onto a CCD camera by doublet lens L2 with focal length  $f = 300$  mm.

The split-and-shift interconnect was formed by first retarding the light to form circular polarization and then using a polarizing beamsplitter to split the wavefronts into two paths. Each of these paths was reflected by mirrors to form a double pass through the retarders so that the two paths were recombined. Finally another retarder circularized the polarizations of this light which was then fed back onto the S-SEED array. A Dove prism (DP) was used in this return path to erect the inverted image without eliminating the image reversion. This prism maybe replaced by an imaging stage or other prism to eliminate the image reversion if desired for other architectural configurations.

Mirrors M1 and M2 were adjusted to provide the two shifts in the interconnect. These shifts were a) vertically down one row and b) vertically up two rows. Thus the three S-SEED rows in this experiment were cyclically imaged onto each other: row 1 onto row 2, row 2 onto row 3, and row 3 back onto row 1 (with spurious interconnects lying outside of the active device region). Since each row was also reversed (side to side) with each imaging stage, the interconnect pattern closed and repeated with every 6 cycles as shown in Figure 8. For example, Figure 8(b) contains a trace of the interconnection path starting at the left most SEED window in row 1. After the first pass through the interconnect, light reflected from this window is incident on the last window in row 2, followed by the first window in row 3, the last window in row 1, etc., until after six passes the light is again incident on the original window.

#### 4.3 Latch Experiment

To verify VCSEL controlled S-SEED operation, a simple latching experiment was performed where neighboring S-SEEDs on the array were set to different output states. This experiment utilized the testbed modules described above with the exception of the interconnect portion of the processor module. As described above, an 8 x 8 array of microlasers were imaged onto a 4x8 portion of the S-SEED array and the output was imaged onto a Videk high resolution camera and framegrabbed. The first window of each S-SEED on the array (odd windows) was taken as the output state of the device. Figure 8 illustrates several four bit data samples from this setup. The four S-SEEDs in the first row comprise the four bit word 0000. To achieve this output, all the microlasers imaged onto even SEED windows were turned on to switch each S-SEED into the low state. These beams were then disabled and the readout module was used to perform readout.

This verified that arbitrary presets of S-SEEDs on a single array was possible with this method.

#### 4.4 Scroll Processor

The scroll processor function is demonstrated by first setting the states of the S-SEEDs to the regular alternating pattern shown in Figure 9(a). Three of the 1 x 8 spot arrays from the Dammann grating are aligned onto three neighboring rows of the S-SEED array, respectively. These three arrays are modulated at 30 kHz with a 30% duty cycle, each out of phase, producing an effective row-to-row scrolling speed of 90 kHz. Thus in the first time step, row 1 is illuminated with the array of power beams while the rows 2 and 3 are dark. During this time the reflected light from row 1 is fed back to row 2 through the "down-1" leg of the interconnect as described above. This returning light sets the state of the devices in the second row. In the second time step, the power beam array for the second row is on, and the states of these devices are read to the third row through the interconnect. Similarly during the third time step the power beams for rows 1 and 2 are off and the row 3 power beams read the state of the row 3 devices onto the row 1 devices through the alternate "up-3" leg of the interconnect.

The operation of this coupled array of three rows of four S-SEEDs is demonstrated in the five CCD photographs in Figure 9 for the case in which the VCSEL imaged onto the sixth window in row 1 (probe VCSEL) was cycled slowly from 0 mW to approximately 0.3 mW and then back to 0 mW. Although the states were clocked from row to row at 30 kHz, these frames show the temporally stable patterns that resulted from scrolling identical states through the array (Figure 9(a)) and then varying the power of this single probe microlaser at a very slow rate (near DC). The behavior of the demonstration scroll

processor is described below, first for the case without the probe VCSEL and then as the probe VCSEL is cycled.

It is readily seen that the pattern shown in Figure 9(a), in which vertical columns of individual SEEDs are alternating low reflectivity (LOW) and high reflectivity (HIGH) is stable in steady state with the interconnect loop described above. For example consider the SEED window in row 1 and column 2 in Figure 9(a). This high reflectivity seed window is imaged onto the low-reflectivity window of the corresponding S-SEED in the next row (row 2, column 7), due to the reversion in the interconnect as described in Figure 2. The relatively high intensity clocked onto this window drives the SEED window it is connected to (row 2, column 8) HIGH. This HIGH window is in turn imaged onto the SEED in row 3 column 1, which drives the SEED in row 3 column 2 HIGH. In this fashion during the sixth pass through the interconnect, the HIGH window in row 3 column 6 is imaged onto the SEED in row 1 column 1, and this repeats the cycle in which the outputs shown in Figure 3(a) are maintained.

An alternate (logic) description of the frame in Figure 3(a) is made by considering each S-SEED as a single device representing a logical 0 when the left window is LOW and 1 when the right window is LOW. In this description it is important to note that the S-SEEDs are inverting devices--in that an S-SEED in state 0, if imaged directly onto another S-SEED with no reversion (i.e., left window onto left window, etc.) will drive the second S-SEED into state 1, and so on. The effect of the reversion described earlier in the interconnect here is to logically re-invert the state of the S-SEED through the interconnect, and so to avoid the high frequency toggle.. Therefore the state of the upper left S-SEED is copied into the last S-SEED in the second row, and so on until after 6 clock steps this state is again read into the upper left S-SEED. In this sense data is

scrolled through the six outer S-SEEDs sequentially and likewise through the six inner S-SEEDs, forming two closed loop scroll paths.

The demonstration experiment continues by slowly cycling on and off the probe VCSEL that illuminates the SEED window in row 1, column 6, starting with the array in the state shown in Figure 9(a). As the probe VCSEL intensity reaches the switching threshold for the S-SEED, this S-SEED is toggled from a state 0 to 1 with the added microlaser intensity on the HIGH window driving it to the LOW state. This new state is then rapidly clocked through the remaining 5 S-SEEDs in the inner scroll path described above. The resulting states in the array are shown in Figure 9(b). While all the S-SEEDs in this inner loop are now in the 1 state (right window LOW) the right window in the S-SEEDs probed is also "bright" due to the light emitted from the probe VCSEL.

As the probe VCSEL intensity increases, the anomalous switching shown in Figure 9(c) is observed. Here the probe VCSEL drives the S-SEED that it illuminates into state 1 as before. This is shown by the high reflectivity of the fifth window in row 1. However the probe VCSEL emits enough power here that even with the higher loss of the LOW window it illuminates, sufficient power from the probe VCSEL passes through the interconnect and switches all the subsequent SEEDs in the inner scroll path to the state 0. As the probe VCSEL power is then reduced, the pattern shown in Figure 9(d) is obtained. This pattern of states is the same as is Figure 9(b), where again all six S-SEEDs in the inner path have returned to state 1 and a small amount of probe microlaser light is still evident.

Finally, as the probe VCSEL is turned completely off, the pattern of states shown in Figure 9(e) is obtained. Here the state 1 has been scrolled through all six S-SEEDs in the inner scroll loop, while the S-SEEDs of the outer scroll loop have maintained their initial

states. Thus, the "pulsing" of the microlaser on the HIGH window of a state 0 S-SEED in the first row toggled it to state 1, and this state was scrolled through the 6-S-SEED loop. In this demonstration sequence only one VCSEL was driven, and it was driven slowly in comparison with the clock rate. If driven at higher rates, the array of VCSELs can be used to set initial states on the S-SEED array, and these states would be cyclically scrolled through their respective loops. Many other scroll loops can be obtained, for example, by eliminating the reversion in the interconnect and/or introducing lateral shifts in the interconnect paths.

## **5.0 Conclusion**

A cascadable scroll processor module has been built as a testbed that demonstrates the use of microlasers as addressable preset devices for S-SEEDs. In principle these VCSELs can be used to combine many masking functions into the VCSEL drivers, arbitrarily preset the individual S-SEEDs in an S-SEED array, and power the S-SEEDs for readout (although Dammann Grating-generated arrays of spots were used for this purpose here). This module also demonstrates the ability to self-cascade processor modules and thus eliminate the need for multiple device arrays. Although system speed and mechanical stability were not stressed in this demonstration, they are important issues of future research.



## Figure Captions

- Figure 1. 3-D optical computing model in which arrays of optical logic gates are connected optically. Fixed masks block light at selected locations to customize system interconnects for specific functions<sup>3</sup>.
- Figure 2. Block diagram and truth table for a 2-to-4 decoder.
- Figure 3. The AT&T 2-to-4 decoder circuit (left) and an equivalent circuit (right).
- Figure 4. Architectural model and gate-level design of a 4 x 1 RAM for the VCSEL/S-SEED processor.
- Figure 5. A 4 x 1 RAM using a fan-out of three.
- Figure 6. A truth table for S-SEED operation using a fan-in of three (left) and a fan-in of four (right).
- Figure 7. S-SEED Based Scroll Processor. The use of microlasers in optical processor modules is studied in this testbed. The processor module contains a single S-SEED array that is fed back onto itself via a split and shift interconnect.
- Figure 8. Scroll Interconnect Pattern. The 6-phase cyclic interconnect pattern used in the demonstration processor is illustrated.
- Figure 9. Experimental Operation. A sequence of 5 CCD photographs show the initial state (a), intermediate stable states (b)-(d), and the final state (e) created by slowly pulsing the microlaser on window 6 in row 1.

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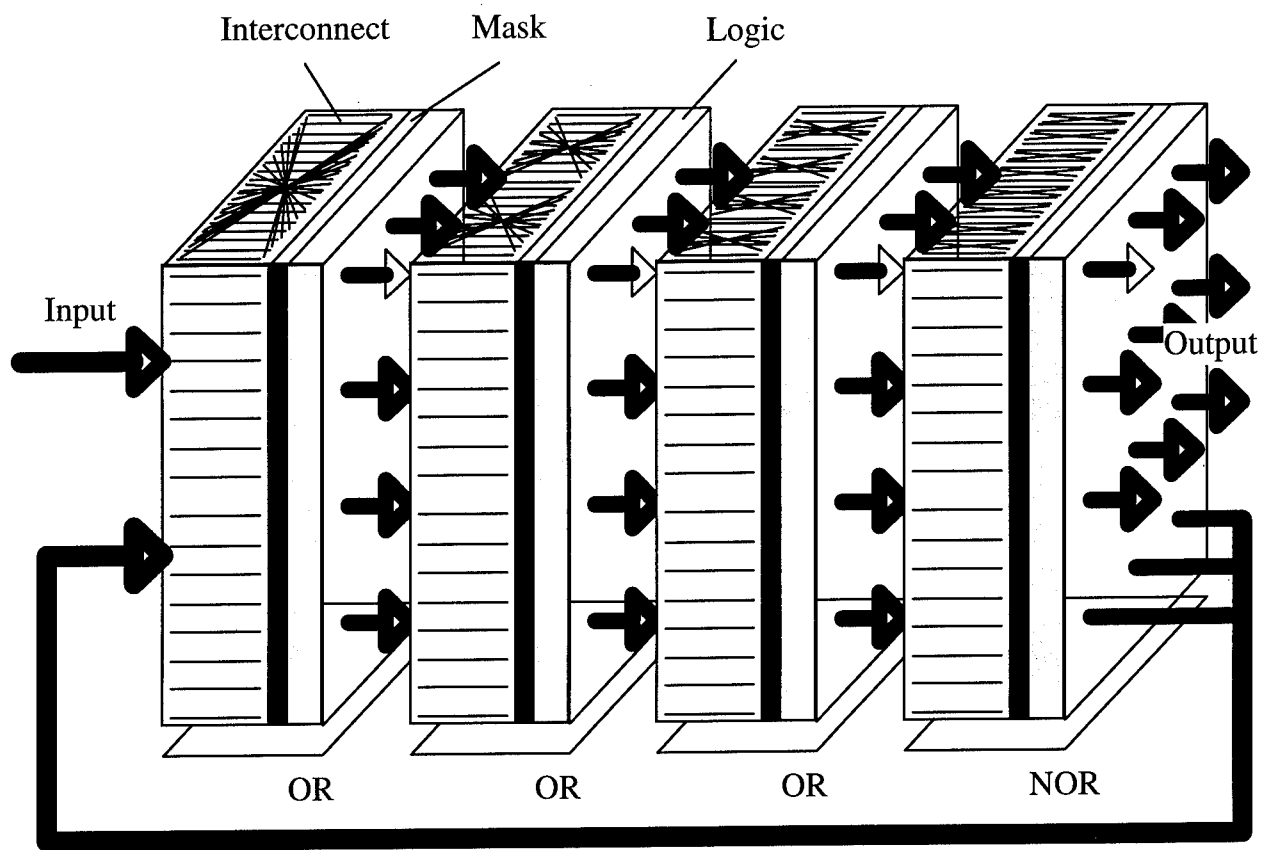
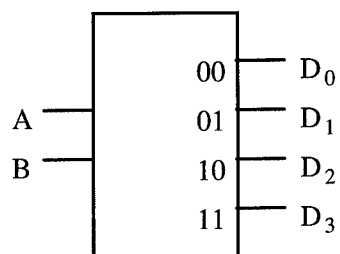


FIGURE 1



A	B	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$$D_0 = \overline{A} \overline{B}$$

$$D_1 = \overline{A} B$$

$$D_2 = A \overline{B}$$

$$D_3 = A B$$

FIGURE 2

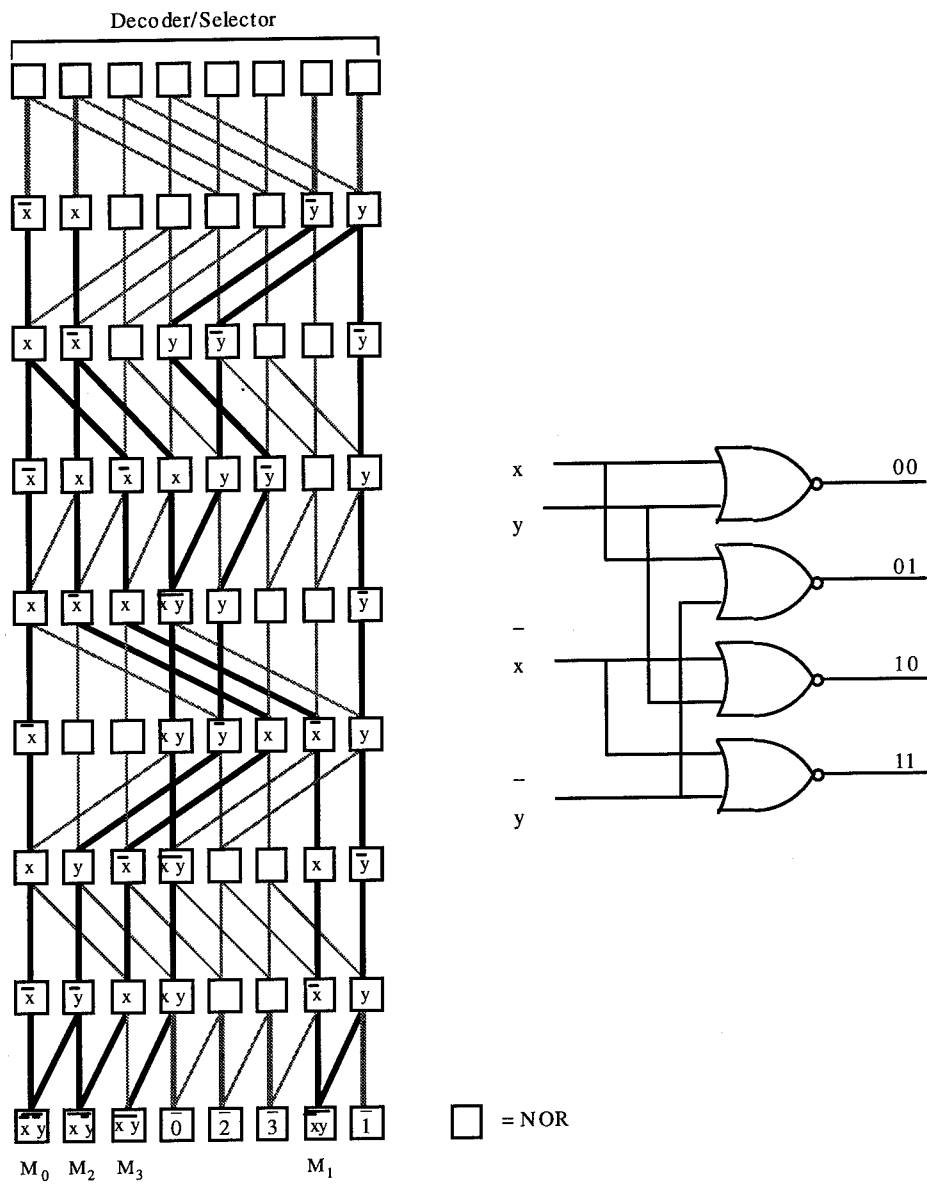


FIGURE 3

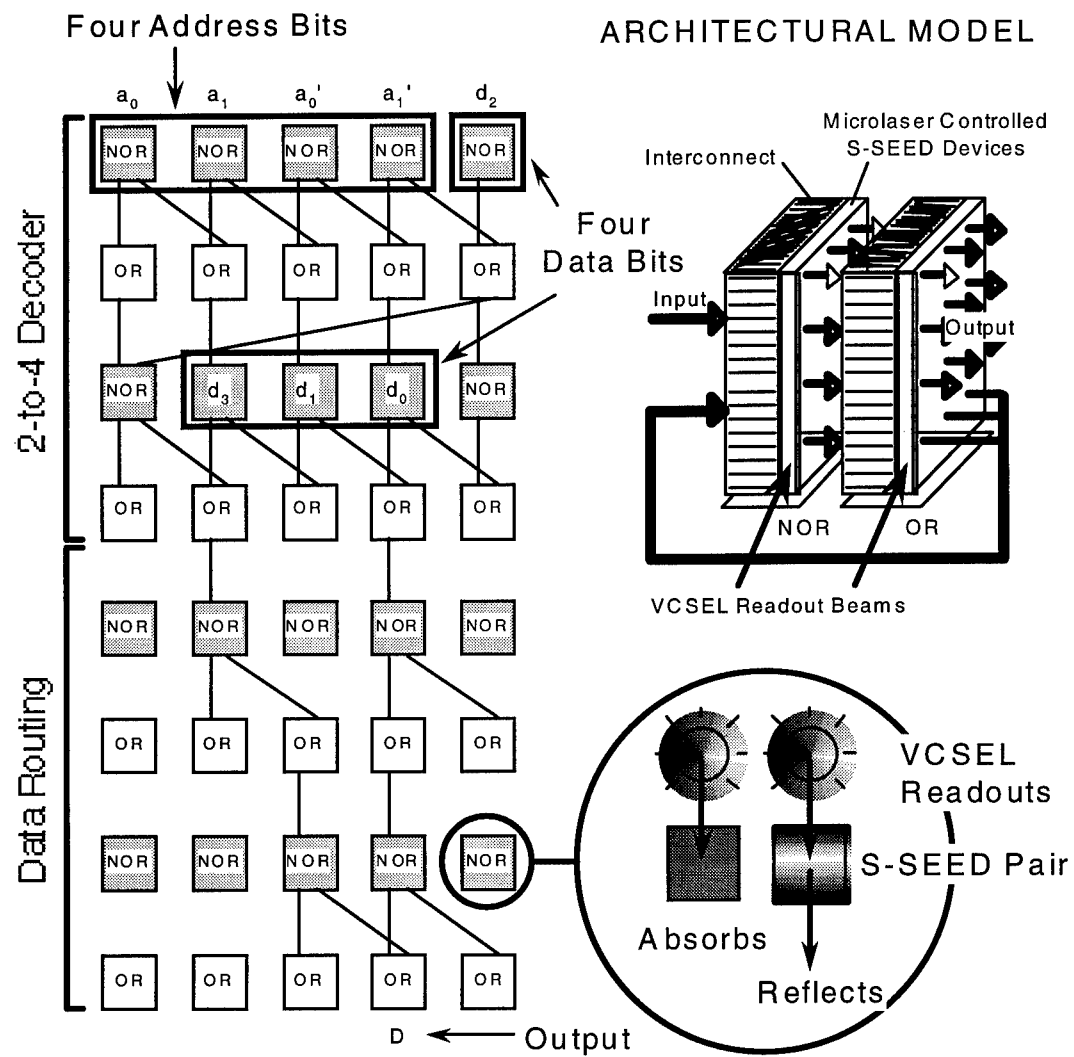


FIGURE 4

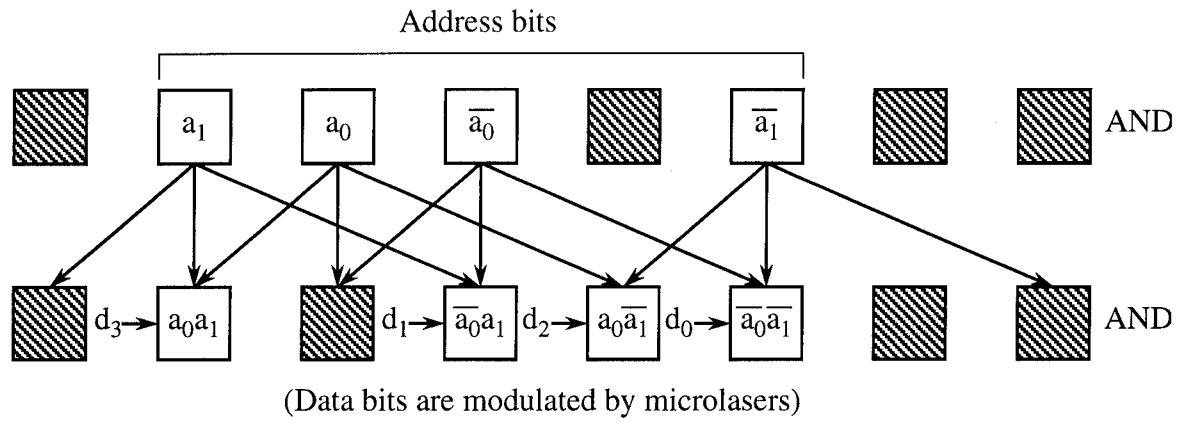


Figure 5



A	B	C	S
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

**Notes:**

S shows the state of the S window in the R-S window pair.

P represents the preset state (either 0 or 1).

A	B	C	D	S
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	P
0	1	0	0	1
0	1	0	1	P
0	1	1	0	P
0	1	1	1	0
1	0	0	0	1
1	0	0	1	P
1	0	1	0	P
1	0	1	1	0
1	1	0	0	P
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

FIGURE 6

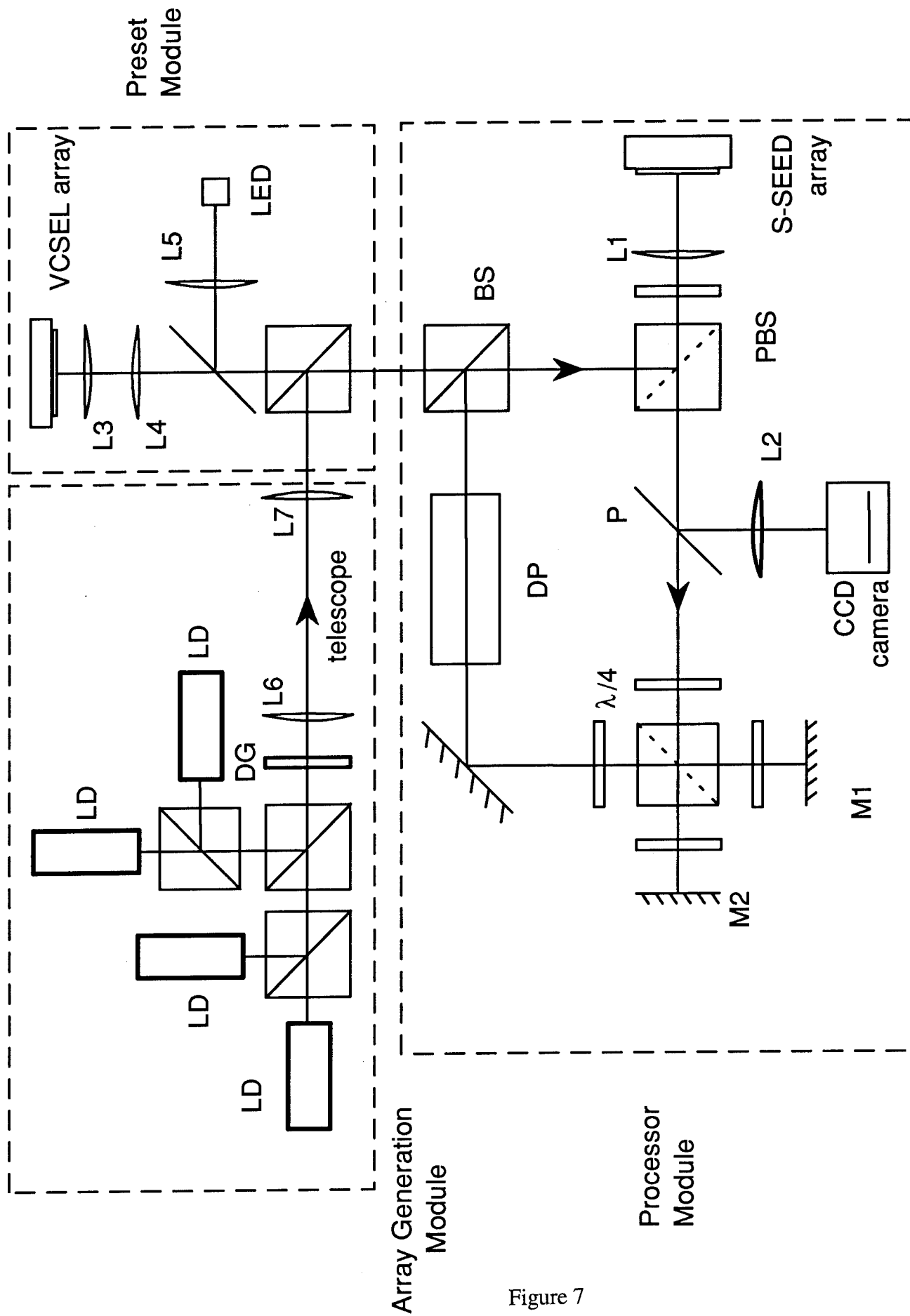
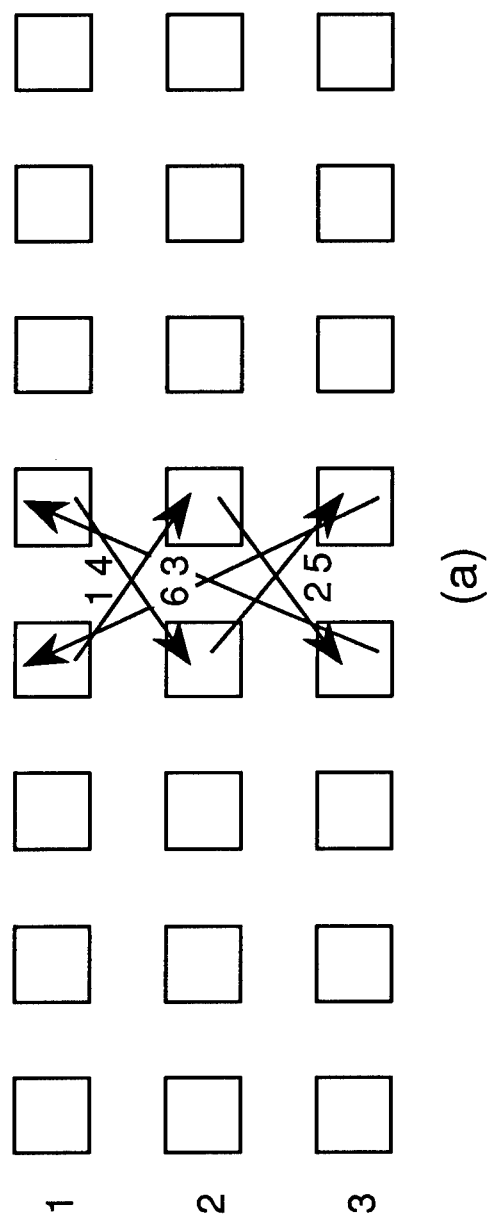
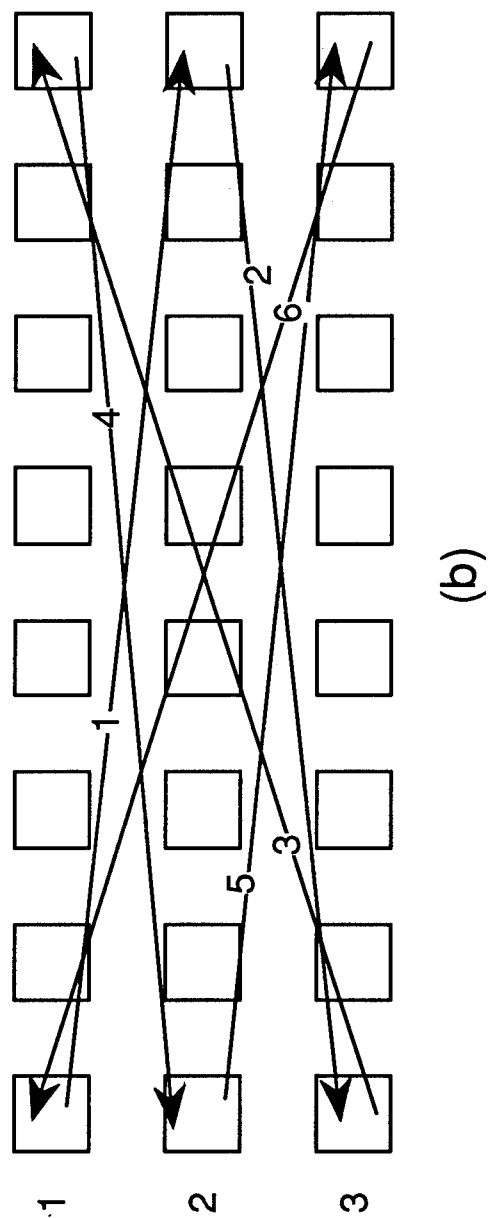


Figure 7



(a)



(b)

Figure 8

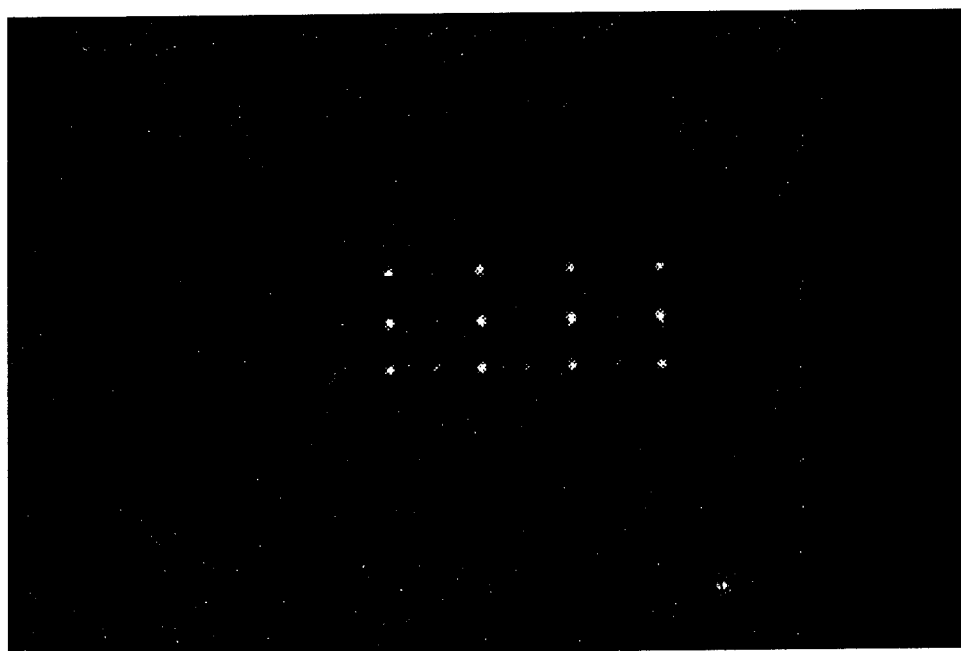


Figure 9a

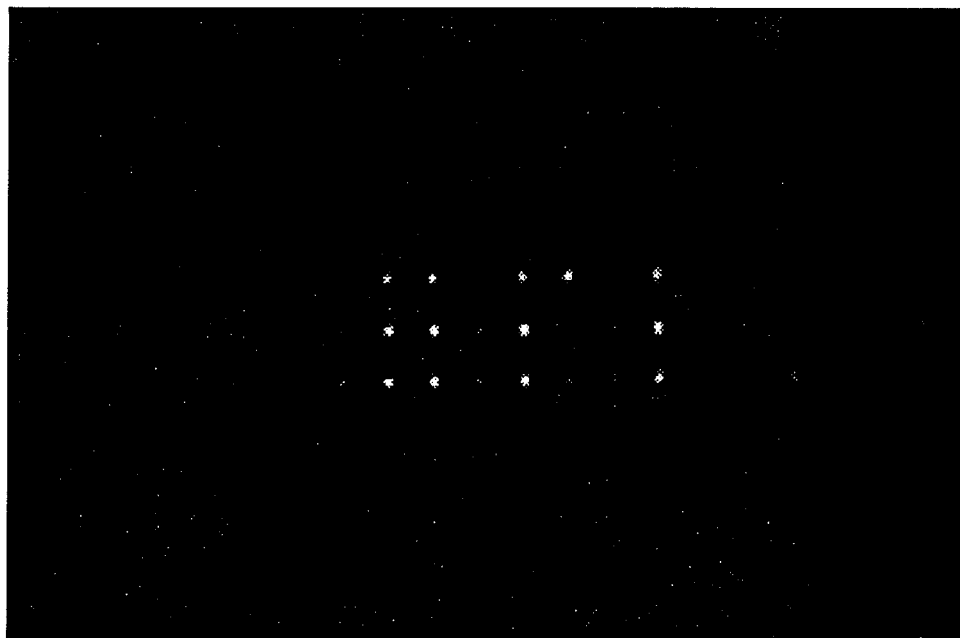


Figure 9b

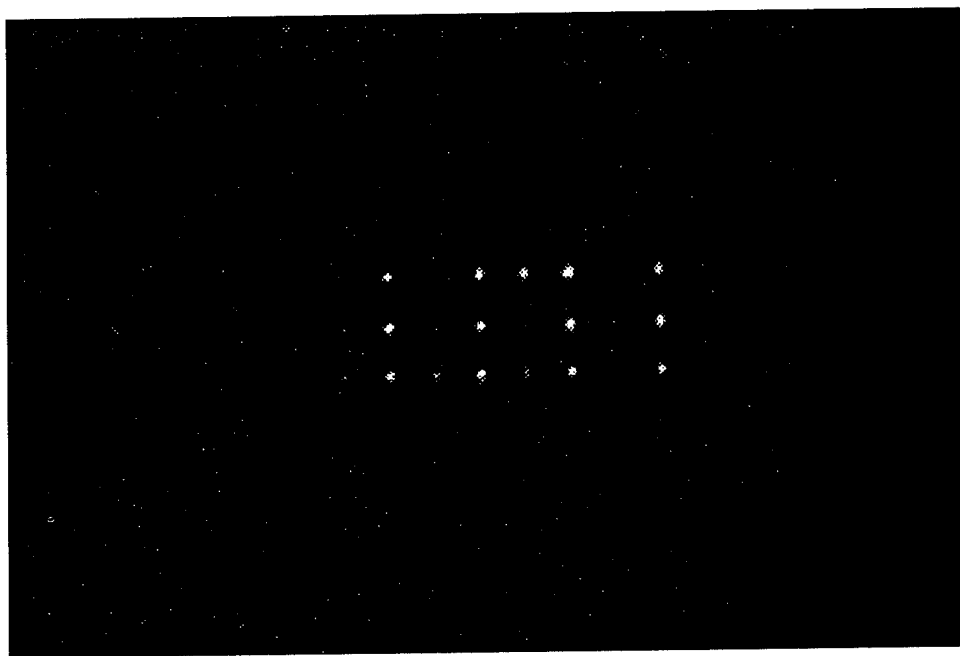


Figure 9c

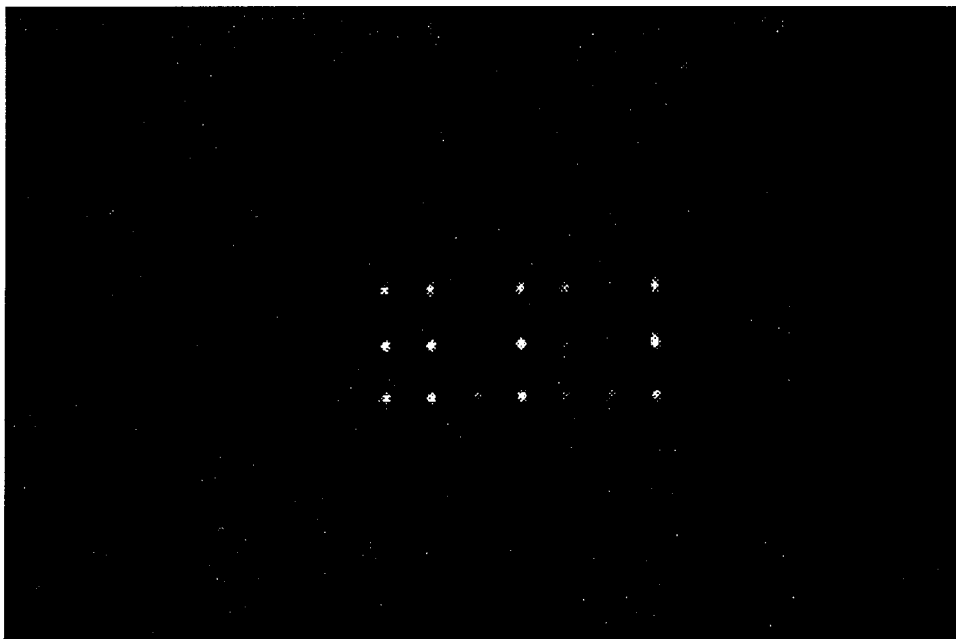


Figure 9d

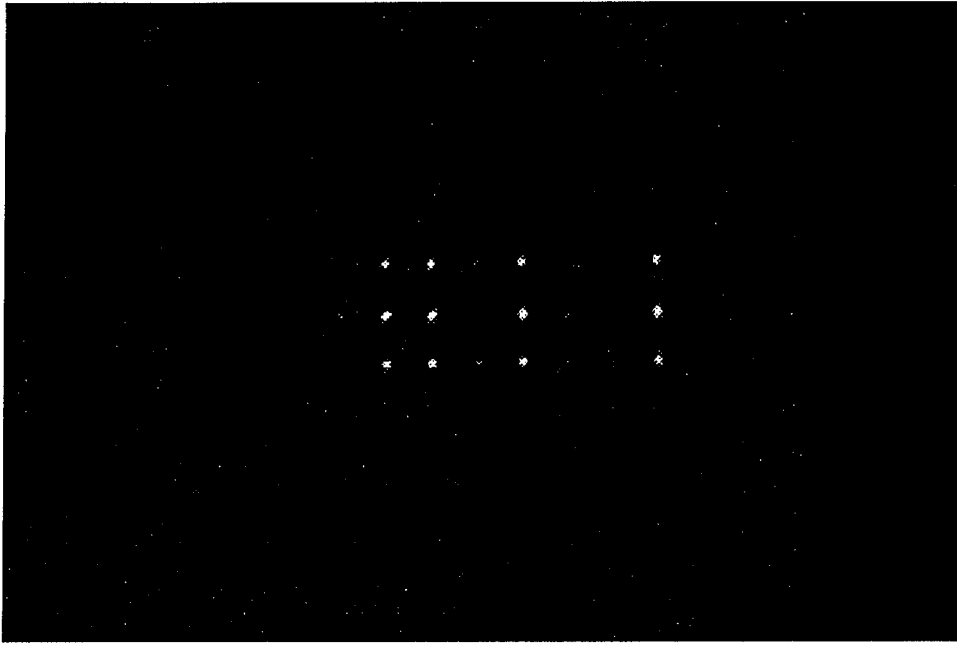


Figure 9e



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